FPGA IMPLEMENTATION OF AN IMPROVED WATCHDOG TIMER FOR SAFETY-CRITICAL APPLICATIONS

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ABSTRACT A watchdog timer is a computer hardware timing device that triggers a system reset if the main program, due to some fault condition, such as a hang, neglects to regularly service the watchdog. The intention is to bring the system back from the hung state into normal operation. Such a timer has got various important applications, one of them being in ATMs which we have studied in our paper. We can implement watchdog timer by using hardware as well as software. The advantage of implement it using software rather than hardware is that it will required less power consumption, less cost and we obtain high speed compare to hardware. The compatible or good known language for Xilinx is VHDL. The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires) and information theory. The simulation tool that we have used is Xilinx 14.5i. Xilinx provide platform for VHDL. First the required code for timer circuit was written in VHDL and simulated so as to obtain the required output waveforms. After the coding was completed, VHDL model is translated into the "gates and wires" that are mapped onto a programmable logic device. The programmable logic device used here is Spartan-III. The above coding and burning methods were completed and the output was observed on FPGA kit. The timer code was implemented using VHDL while burning was done using Spartan-III kit.

Keywords: ATM (Automated Teller Machine), CLB(Configurable Logic Blocks), DLL (Delay Locked Loops), DRC (Design Rule Checker), EMI (Electromagnetic Interference), FPGA(Field Programmable Gate Array),VHDL (Very High Speed Integrated Circuits Hardware Description Language), VLSI (Very Large Scale Integration).

1. INTRODUCTION Today, microcontrollers are being used in tough environments where electrical noise and EMI are plentiful. In environments like this, it is beneficial if the system contains resources to help ensure proper operation. In many systems, a

commonly used technique for verifying proper operation is the combination of a watchdog timer. A watchdog timer is fundamentally a time measuring device that is used in conjunction with or as part of a microprocessor and is capable of causing the microprocessor to be reset. A system using a watchdog timer is particularly well suited to detecting bit errors. Momentary bit errors can be caus ed by such things as soft memory failures and electromagnetic discharges into memory devices and their interfaces. These can cause temporary bit polarity flipping of data into and out of the processor. When this occurs while fetching program information, t he microprocessor will begin executing invalid code. The most common use of the High-Speed Micro's watchdog timer is as a system supervisor [5]. VHDL is a hardware description that can be used to model a digital system. The hardware abstraction of this digital system is known as ENTITY. To describe an entity, VHDL provides five different types of primary construct, called as design units. They are: Entity declaration, Architecture body, Configuration declaration, Package declaration and Package body. Architecture body consist of three types of modeling which are structural, dataflow and behavioral. Behavioral style of modeling specifies the behavior of an entity

as a set of statement that are executed sequentially. All the flow of program is executed sequentially, which is the function of behavioral modeling. As VHDL provides an extensive range of modeling capabilities, it is possible to quickly assimilate a core subset of the language that is both easy and simple to understand without learning the complex features [3-4]. FPGA is a semiconductor device containing programmable logic components and programmable interconnects .The programmable logic components can be programmed to duplicate the functionality of basic logic gates such as AND, OR, XOR, NOT or more complex combinational functions such as decoders or simple mathematical functions. The advantages of FPGA are that it is shorter time to market,ability to re-program in the field to fix bugs and lower non recurring engineering costs. The typical basic architecture consists of an array of CLBs and routing channels. Multiple I/O Pads may fit into the height of one row or the width of one column in the array. Generally, all the routing channels have the same width (number of wires). An application circuit must be mapped into an FPGA with sufficient resources [5]. The Spartan-II 2.5V FPGA family gives users high performance, rich logic resources, and a

rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates. System performance is supported up to 200 MHz Spartan-II devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined Virtex - based architecture. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements. The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary.

2. LITERATURE SURVEY

VLSI system can be implemented with the help of back-end as well as front-end tools. Approach of good designer towards in front-end is because of number of advantages over back-end tools like: Logical approach is more in front-end as compare to back- end, syntax rules are present in front-end whereas in back-end DRC rules are present , front-end is

more flexible that means we can edit it fast but back-end is not that much flexible [1-2]. Hence we are implementing watchdog timer with the help of front end-tool that is Xilinx To implement the watchdog timer we can use different languages like assembly, Verilog… etc, but VHDL is the most powerful language as well as different modeling techniques can use so as to improve flexibility and performance of the system. Different modeling techniques of VHDL are Dataflow, Structural and Behavioral. In our implementation we are using behavioral modeling due to it's sequential execution and program syntax is easy as compare to dataflow and structural modeling [3-4]. We can use Altera, Atmel and Cortex-M are front end tools but that are used in industry level applications but Xilinx is used at academic level which is easy to understand at student level.

CONVENTIONAL CODE

In beginning days ATM machines was built by conventional codes such as C, C++ which can be simply tracked by intruders. It can be modified and corrupted with effortlessly and low level of complications. Also, the conventional codes are simulated through a numbers of blocks and then it can be implemented at the ATM machine. To

overcome these problems by using suitable VHDL (Very High Speed Integrated Circuit Hardware Description Language) codes instant of conventional source coding. The complete transaction process involving the various ATM functions are implemented using VHDL, as it is a more protected programming language and permits for a better design management. Also, VHDL is technology independent. The ultimate result of the coding is observed by integrating it on the Spartan FPGA Kit. VHDL is an atomic hardware description language which can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the entry level. The digital system can also be described powerful language tool worked hierarchical mannertiming signal can also be obviouslymodelled in the same description. VHDL is a powerful language with abundant languages constructs that re capable of describing very complex performance.In general there are two types of ATM machines are available based on their operation.

The types are, 1. Leased-line ATM 2. Dial-up ATM machines The types of machines can be differing based on the input terminal with dual inputs and four output devices on the availability of a host processor. The host processor is very important part that needs to connect and also communicate with the person ask for the money. At the same time Internet Service Provider (ISP) also plays a significant role in this action. They act as the gateway to the intermediate networks and also the bank computer.

The automatic teller machine is also called as an automatic banking machine (ABM) which permitsto accuse customer's basic transactions without any help of bank legislative body. At present there are two types of automatic teller machines (ATMs) are available. The basic one agrees the customer to only draw cash and collect a report of the account balance. Second one is a more complex machine which receives the deposit, offers A leased-line ATM machine has been connecting it with the host processor with the help of 4-wire point to point devoted telephone line. These types of machines are widely used where the user volume is high. So that it can be considered as high end and the operating costs is also very high. The dial-up ATM machines are like a usual phone line with a modem and a toll free number. In this type of normal connection setup their initial installation cost is very less and their operating costs only become a portion of that of a leased-line ATM.The host machines are usuallymaintained by the bank and also owned by an ISP. If the host is only

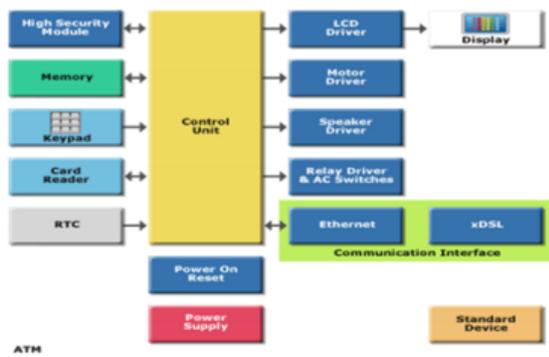maintained by the bank that machines will be supportedfor that particular bank does not support other bank cards.

Fig: 2 Block diagram

VHDL CODE IMPLEMENTATION

VHDL is digital descriptive language for electronic systems. VHDL is a complex coding simulation language hard to implement in ATM machine it provide wide range security in money transfer. The block diagram of ATM credit card payment services and reports account information.In which the use of computer to transfer debits and credits with the help of electronic pulses, which are passed through wire either to a magnetic disk or tape. Using an ATM card a customer can access approximately all the facilities available from a counter service. Flow chart of one session diagram is shown in figure 3.

The basic operation rendering to the flowchart can be describedas the following stages. In initial stage, the customer should insert the card at the slot provided for card insertion in the ATM

machine for card authentication. The card reader is an input device that reads information from a card. The magnetic strip on the back side of the ATM card is used to connect with the card reader it is used to identify the particular account number and transfer the data from the card to the host processor (server). The host processor collects the information from the bank.

In second stage customer required to enter their personal identification number. Each card has unique PIN number so that can withdraw money from there account. There are separate laws to protect the PIN code while sending it to host processor. The PIN number is mostly sent in encrypted from. The key board contains 48 keys and is interfaced to the processor.
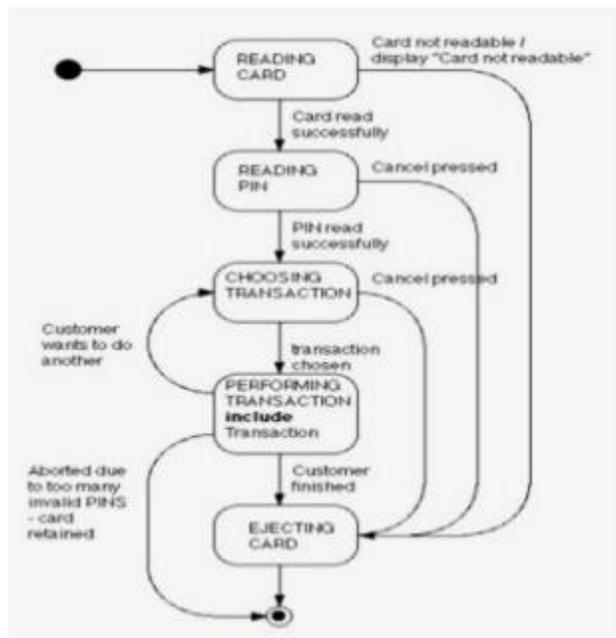

Fig. 2 One session flow chart

If the pass ward entry was successfully entered in machine the display screen displays the transaction information. Customer need to choose their account type either savings account or current account. If the person chose savings account, the moneywithdrawal is done on the Savings Account else the money is withdrawn from the Current Account. After complete their transaction the customer need to logout the session.
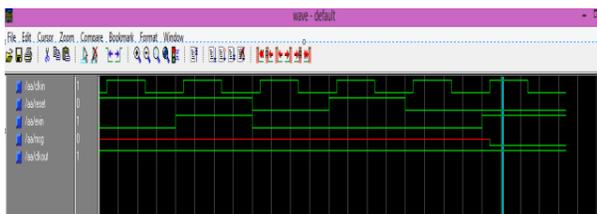
RESULT WITH DISCUSSION

Figure 4: Result

We have given 3 input signals clkin, reset and exin. Clkout signal remains 1 as per condition given in program. We have also use a xu as a user defined signal. The xu signal can be incremented at the rising edge of the clkin signal. The message signal which is a output signal which depends on xu signal. The xu signal counts from 22 downto 0, which will then reset our watchdog timer if any fault condition occurs.

CONCLUSIONS AND FUTURE SCOPE

As VHDL provides an wide range of modeling capabilities, it is possible to quickly integrate a core subset of the language that is both easy and simple to understand without learning the complex features. We successfully implemented a timer for ATM application and observed its output, both as test bench waveform an d on Spartan-II kit. The scope of this paper or project to be simulate the Watchdog timer using different simulation tools like Atmel, Altera and Cortex-M. VHDL codesimprove the ATM security compare to conventional coding. In this article we explained the working principle and security terms to improve the ATM service. VHDL is a new technology which may prove to be highly useful and provide more efficient banking service.

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